REMARKS/ARGUMENTS

Claims 1-20 are pending in the present application. With this amendment, claims 1, 3, 5-7, 9-10, 12, 14-16, and 18-20 were amended. Reconsideration of the claims is respectfully requested.

I. Examiner Interview

Applicant appreciates the courtesies extended by the Examiner in the interview that was conducted on January 19, 2007. Applicant's claims and the cited prior art were discussed. No agreement was reached.

II. Claim Objections

The Examiner objected to claims 1-20 because of informalities.

Specifically, the Examiner stated that it is not clear what is meant by pulses that are a first and second length. The Examiner also stated that it is unclear what "logical ones using pulses that are a first length" and what "logical zeros pulses that are a second length" comprises.

Applicant has amended claims 1, 10, and 19 to describe indicating logical ones using first pulses that are a first width and indicating logical zeros using second pulses that are a second width. Applicant's specification describes a pulse length and a pulse width as being the same thing. See Applicant's specification page 14, line 9.

The Examiner also stated that it is unclear how "data" is interrelated and associated with "logical ones" and "logical zeros". Applicant has amended claims 1, 10, and 19 to describe configuring the I/O pin to be used to transmit and receive pulses.

Applicant believes the objections to the claims have been overcome by the amendments to the claims and should be withdrawn.

III. 35 U.S.C. § 102(a), Anticipation

The Examiner has rejected claims 1, 3, 8-10, 12 and 19 as being anticipated by *Frankowsky,* On Chip Programmable Data Pattern Generator for Semiconductor Memories, U. S. Patent No. 6,651,203 (November 18, 2003). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicant's claim 1 recites "configuring said I/O pin to be used to transmit and receive pulses, indicating logical ones using first pulses that are a first width and indicating logical zeros using second pulses that are a second width; and communicating with said device by transmitting and receiving said

first and second pulses via said I/O pin." Thus, the first pulses are a first width and the second pulses are a second width.

Applicant's Figure 3 depicts first and second pulses. A pulse is a transient change in the amplitude from a baseline. In Figure 3, the baseline is indicated by reference number 306. Bit stream 300 illustrates four pulses. These pulses indicate a logical 0, followed by three logical 1s. All pulses in bit stream 300 have the same amplitude.

Although each pulse has the same amplitude, the width of the pulses varies depending on whether the pulse indicates a logical 1 or a logical 0. For example, the width of the first pulse, which indicates a logical 0, has a width that is different from the width of the second, third, and fourth pulses, which each indicate a logical 1. This is shown using reference numbers 302 and 304, which depict different widths. Reference number 302 indicates the width of a pulse that indicates a logical 0. Reference number 304 indicates the width of a pulse which indicates a logical 1. As depicted in Figure 3, the width of a pulse that indicates a logical 0 is smaller than the width of a pulse that indicates a logical 1.

The Examiner stated:

> As to claims 1, 10,12, Frankowsky discloses an apparatus for testing the memory device (1 02) with a plurality of I/O pins (DQ) as shown in figure 2 having at least one input/output pin (DQ) configured to be used to transmit and receive data, an external device (,110,108) for communicating with the device (102) utilizing logic signal (one "high" or low "zero") (see column 4, lines 20-3 1) by transmitting the logic signal to the device utilizing the 1/0 pin (DQ). It appears that the logical ones (high) in the device of Frankowsky inherently use pluses[sic] that are a first length and a logical zeros (low) in the device of Frankowsky inherently use pulses that are a second length.

Office Action dated October 30, 2006, pp. 2-3.

Frankowsky teaches using charged and discharged capacitors to produce the bit patterns depicted in *Frankowsky's* Figures 1A-1C. To test a chip, a well-know data pattern is written to the chip and then read back. These data patterns are described in *Frankowsky* in column 1, lines 35-57. These data patterns include combinations of changed and discharged capacitors to indicate a physical 1 data pattern, a logical 1 data pattern, or a checkerboard data pattern.

Frankowsky also describes using these data patterns in its pattern generator.

> Memory address lines 120 include row address lines and column address lines. Memory address lines 120 supply locations within memory 114 of memory cells to be written from by pattern generator 108 to memory cells 106 of array 102. Pattern generator 108 manages the address information to write pattern data to memory cells 106 in accordance with the pattern specified, for example, a physical pattern (see FIGS. 1A and 1C) or a logical pattern (see FIG. 1B), and the pattern data. The pattern topology (physical data scrambling or arrangement of data within memory array 102) is controlled by a subset of row and column addresses supplied to pattern generator 108 through row lines and column lines of memory address lines 120. In one embodiment, only a single bit

> (1 or 0) is needed on row lines of memory address lines 120 to provide row address data scrambling as illustrated in FIG. 1. Two or three bits (1s and/or 0s) may be needed on column lines of memory address lines 120 to provide column address data scrambling as illustrated in FIG. 1. The actual number of bits for row/column data scrambling may be varied according to the chip architecture.

Frankowsky, column 4, lines 43-62.

Frankowsky does not teach pulses that have different widths. Nothing in *Frankowsky* describes different widths. *Frankowsky* merely teaches determining a state of a capacitor, i.e. whether it is charged or discharged.

In fact, the Examiner does not point to anything in *Frankowsky* that teaches pulses having different widths. The Examiner finds that such a teaching must be inherent in *Frankowsky*, but does not find any such teaching in *Frankowsky*.

Because *Frankowsky* does not teach indicating logical ones using first pulses that are a first width and indicating logical zeros using second pulses that are a second width, *Frankowsky* does not anticipate Applicant's claims. Furthermore, because *Frankowsky* does not teach indicating logical ones using first pulses that are a first width and indicating logical zeros using second pulses that are a second width, *Frankowsky* does not teach communicating with said device by transmitting and receiving said first and second pulses via said I/O pin.

Therefore, the rejection of claims 1, 3, 8-10, 12 and 19 under 35 U.S.C. 102(a) has been overcome.

IV. Objection to Claims

The examiner has stated that claims 2, 4-7, 11-18 and 20 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

V. Conclusion

It is respectfully urged that the subject application is patentable over *Frankowsky* and *Dukes* and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: January 29, 2007

Respectfully submitted,

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